WHAT IS CLAIMED IS:

1. A multiprocessor system comprising a first processor and a second processor, wherein:

the first processor includes an interrupt generation unit which generates an interrupt to the second processor when the first processor executes a predetermined call instruction in a running main routine; and

the second processor includes an address save unit which saves a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction to a predetermined memory area when the second processor receives an interrupt from the interrupt generation unit.

2. The multiprocessor system according to claim 1, wherein:

the interrupt generation unit generates an interrupt to the second processor again when a predetermined return instruction is executed in the subroutine; and

the second processor further includes an address notification unit which notifies the return address to the first processor when receiving the re-generated interrupt.

3. The multiprocessor system according to claim 1, wherein

the first processor includes a fetcher which fetches an instruction; and the return address is set as a target address to be accessed by the fetcher.

4. A multiprocessor system comprising a first processor and a second processor, wherein:

the first processor includes an interrupt generation unit which generates an interrupt to the second processor when the first processor executes a predetermined call instruction or jump instruction; and

the second processor includes:

an address extraction unit which extracts a call destination address or jump destination address stored dividedly in formats of the call instruction or the jump instruction and an accompanying execution stop instruction when the second processor receives the interrupt from the first processor; and

an address notification unit which notifies the acquired call destination address or jump destination address to the first processor.

5. The multiprocessor system according to claim 4, wherein:

the first processor includes a fetcher which fetches an instruction; and

the call destination address or the jump destination address is set as a target address to be accessed by the fetcher.

6. A multiprocessor system comprising a graphics processor and a main processor, wherein

the graphics processor includes:

a direct memory access controller (DMAC) which reads instructions written in a display list from a memory in succession;

a decoder which decodes the read instructions in succession; and

an interrupt generation unit which generates a shift interrupt to the main processor when a decoded instruction is a predetermined call instruction included in a main routine of the display list and generates a return interrupt to the main processor when a decoded instruction is a return instruction included in a subroutine called by the call instruction,

the main processor includes:

an address save unit which saves a return address for returning to the main routine upon completion of processing of the subroutine to a predetermined memory when the main processor receives the shift interrupt from the interrupt generation unit; and

an address notification unit which reads the return address from the predetermined memory and notifies the return address to the graphics processor when the main processor receives the return interrupt from the interrupt generation unit, and

the return address notified to the graphics processor is set as a target address to be accessed by the DMAC.

7. A multiprocessor system comprising a graphics processor and a main processor, wherein

the graphics processor includes:

a direct memory access controller (DMAC)which reads instructions written in a display list from a memory in succession;

a decoder which decodes the read instructions in succession; and

an interrupt generation unit which generates an interrupt to the main processor when a decoded instruction is a predetermined call instruction or a jump instruction included in the display list,

the main processor includes an address notification unit which acquires a call destination address or a jump destination address stored dividedly in formats of the call instruction or the jump instruction and an accompanying execution stop instruction, and notifies the call destination address or the jump destination address to the graphics processor when the main processor receives the interrupt from the interrupt generation unit, and

the call destination address or the jump destination address notified to the graphics processor is set as a target address to be accessed by the DMAC.

8. A method of executing a program in a multiprocessor system, the method comprising, when a first processor executes a call instruction in a running main routine, committing save of a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction to a second processor.

9. The method of executing a program in a multiprocessor system according to claim 8, wherein:

if a stack area inside the first processor has a free space, the first processor saves the return address to the stack area by itself; and

if the stack area has no free space, the save of the return address is committed to the second processor.

10. The method of executing a program in a multiprocessor system according to claim 8, wherein:

if the call instruction does not explicitly instruct to commit the save of the return address to the second processor, the first processor saves the return address to a stack area built in itself; and

if the call instruction explicitly instructs to commit the save of the return address to the second processor, the first processor commits the save of the return address to the second processor.

11. A method of executing a program in a multiprocessor system, the method comprising, when a first processor executes a call instruction or jump instruction, committing acquisition of a call destination address or a jump destination address to a second processor if the number of bits of the call destination address or jump destination address exceeds the number of bits acquirable by the first processor.

12. A method of executing a program in a multiprocessor system, the method comprising, when a first processor executes a call instruction or a jump instruction, committing acquisition of a call destination address or jump destination address to a second processor if the call instruction or the jump instruction explicitly instructs to commit the acquisition of the call destination address or the jump destination address to the second processor.